WE CLAIM

1. A print engine controller for a pagewidth printhead having at least one printhead chip that spans a print area, the controller being connectable to a memory device, a micro-processor and the, or each, printhead chip, the controller comprising

control circuitry for permitting external clients to read and write registers and to read and write to the memory device;

a data bus that is connectable to the memory device;

a data interface that is connected to the data bus to be interposed between the data bus and the microprocessor, in use, so that the microprocessor can write data to the memory device;

a serial interface that is connected to the data bus to be interposed between the data bus and the micro-processor, in use, so that the micro-processor can access the registers of the control circuitry and registers of the memory device;

page expansion circuitry that is connected to the data bus and is configured to receive data representing compressed pages and to render that data into dot data representing dots;

formatting circuitry that is connected to the data bus for receiving the dot data and for formatting the dot data for printing; and

a printhead interface that is interposed between the formatting circuitry and the printhead chips, in use, to receive the dot data from the formatting circuitry and to communicate the dot data to the printhead chips.

2. A print engine controller as claimed in claim 1, in which the control circuitry is configured to permit the reading and writing of data in 32 bit data blocks.

3. A print engine controller as claimed in claim 1, which includes a random access memory device controller that is connectable to the memory device, which is a random access memory device, such that, in use, the memory device controller is interposed between the memory device and the data bus, a memory device interface being interposed between the memory device controller and the data bus.

4. A print engine controller as claimed in claim 1, in which the serial interface is a low speed serial interface.

5. A print engine controller as claimed in claim 1, in which the page expansion circuitry is configured to render the compressed page data into bi-level dot data.

6. A print engine controller as claimed in claim 1, in which the data interface is a high-speed interface.

7. A print engine controller as claimed in claim 1, in which the formatting circuitry is configured to format the dots for predetermined print lines.